WHAT IS CLAIMED IS:

1. A semiconductor device characterized in comprising:

a wiring layer formed on a main surface of a semiconductor chip; and

a conductive layer for interlayer connections that is connected to the wiring layer and formed in a side wall of the semiconductor chip.

2. A semiconductor device characterized in comprising:

electrode pads formed on a main surface of a semiconductor chip;

grooves formed in a section of the semiconductor chip that traverses in a thickness direction of the semiconductor chip;

conductive layers filled in the grooves; and

wiring layers that connect the electrode pads and the conductive layers.

3. A semiconductor module characterized in comprising:

semiconductor chips stacked in layers;

conductive layers that are formed in side walls of the respective semiconductor chips for providing interlayer connections among the semiconductor chips; and

wiring layers that are formed on main surfaces of the respective semiconductor chips and connected to the conductive layers.

4. A semiconductor module characterized in comprising:

semiconductor chips stacked in layers;

electrode pads formed on main surfaces of the respective semiconductor chips;

grooves that are formed in sections of the respective semiconductor chips that traverse in a thickness direction of the semiconductor chips;

conductive layers filled in the grooves for providing interlayer connections among the semiconductor chips; and

wiring layers that connect the electrode pads and the conductive layers, respectively.

5. A semiconductor module characterized in comprising:

semiconductor chips stacked in layers;

electrode pads formed on main surfaces of the respective semiconductor chips;

grooves that are formed in sections of the respective semiconductor chips that traverse in a thickness direction of the semiconductor chips;

wiring layers that connect the electrode pads and the conductive layers;

pin-like terminals that are embedded in the grooves and disposed in a stacking direction of the semiconductor chips;

an interposer substrate with the pin-like terminals standing thereon; and

conductive layers filled in the grooves with the pin-like terminals therein.

6. A semiconductor module according to claim 3, characterized in that the semiconductor chips are stacked in layers through dielectric resin.

7. A semiconductor module characterized in comprising:

an interposer substrate having a wiring layer formed on a main surface thereof;

a semiconductor chip that is connected to the wiring layer and mounted on the interposer substrate;

grooves formed in a side wall of the interposer substrate that traverses in a thickness direction of the interposer substrate; and

conductive layers filled in the grooves.

8. A semiconductor module characterized in comprising:

interposer substrates stacked in layers;

wiring layers formed on main surfaces of the interposer substrates;

semiconductor chips that are connected to the wiring layers and mounted on the interposer substrates;

grooves formed in side walls of the interposer substrates that traverse in a thickness direction of the interposer substrates;

conductive layers filled in the grooves for providing interlayer connections among the interposer substrates; and

recessed sections formed in back surfaces of the interposer substrates for storing the semiconductor chips.

9. A semiconductor module characterized in comprising:

an intermediate substrate having an opening section formed therein;

interposer substrates stacked in layers through the intermediate substrate;

wiring layers formed on main surfaces of the interposer substrates;

semiconductor chips that are connected to the wiring layers and mounted on the interposer substrates;

first grooves formed in side walls of the interposer substrates that traverse in a thickness direction of the interposer substrates;

second grooves formed in a side wall of the intermediate substrate that traverses in a thickness direction of the intermediate substrate; and

conductive layers filled in the first grooves and the second grooves for providing interlayer connections among the interposer substrates through the intermediate substrate.

10. An electronic device characterized in comprising:

semiconductor chips stacked in layers;

electrode pads formed on main surfaces of the respective semiconductor chips;

grooves that are formed in sections of the respective semiconductor chips that traverse in a thickness direction of the semiconductor chips;

conductive layers filled in the grooves for providing interlayer connections among the semiconductor chips;

wiring layers that connect the electrode pads and the conductive layers, respectively; and

an electronic component that is connected to the semiconductor chips through the conductive layers.

11. An electronic device characterized in comprising:

semiconductor chips stacked in layers;

electrode pads formed on main surfaces of the respective semiconductor chips;

grooves that are formed in sections of the respective semiconductor chips that traverse in a thickness direction of the semiconductor chips;

wiring layers that connect the electrode pads and the conductive layers, respectively;

pin-like terminals that are inserted in the grooves and disposed in a stacking direction of the semiconductor chips;

an interposer substrate with the pin-like terminals standing thereon;

conductive layers filled in the grooves with the pin-like terminals therein; and

an electronic component that is connected to the semiconductor chips through the conductive layers.

12. An electronic device characterized in comprising:

interposer substrates stacked in layers;

wiring layers formed on main surfaces of the interposer substrates;

semiconductor chips that are connected to the wiring layers and mounted on the interposer substrates;

grooves formed in side walls of the interposer substrates that traverse in a thickness direction of the interposer substrates;

conductive layers filled in the grooves for providing interlayer connections among the interposer substrates;

recessed sections formed in back surfaces of the interposer substrates for storing the semiconductor chips; and

an electronic component that is connected to the semiconductor chips through the conductive layers.

13. An electronic device characterized in comprising:

an intermediate substrate having an opening section formed therein;

interposer substrates stacked in layers through the intermediate substrate;

wiring layers formed on main surfaces of the interposer substrates;

semiconductor chips that are connected to the wiring layers and mounted on the interposer substrates;

first grooves formed in side walls of the interposer substrates that traverse in a thickness direction of the interposer substrates;

second grooves formed in a side wall of the intermediate substrate that traverses in a thickness direction of the intermediate substrate;

conductive layers filled in the first grooves and the second grooves for providing interlayer connections among the interposer substrates through the intermediate substrate; and

an electronic component that is connected to the semiconductor chips through the conductive layers.

14. A method for manufacturing a semiconductor device, characterized in comprising:

a step of forming through holes on cutting lines of a semiconductor wafer;

a step of cutting the semiconductor wafer along the cutting lines into chips; and

a step of filling conductive layers in the through holes divided by the cutting step.

15. A method for manufacturing a semiconductor device, characterized in comprising:

a step of forming trench sections on cutting lines of a semiconductor wafer having wiring layers formed thereon;

a step of forming dielectric films within the trench sections;

a step of forming an under barrier metal layer that covers the dielectric films and is connected to the wiring layers;

a step of thinning a back surface of the semiconductor wafer to thereby make the trench sections penetrate to form through holes along the cutting lines;

a step of cutting the semiconductor wafer along the cutting lines into chips; and

a step of filling conductive layers in the through holes that are divided by the cutting step.

16. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming conductive layers on side walls of a semiconductor chip; and

a step of providing interlayer connections through the conductive layers formed on the side walls of the semiconductor chip.

17. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming through holes on cutting lines of a semiconductor wafer;

a step of cutting the semiconductor wafer along the cutting lines into chips;

a step of stacking the semiconductor chips formed by the cutting step; and

a step of filling conductive layers in the through holes cut by the cutting step.

18. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming through electrodes on cutting lines of a semiconductor wafer;

a step of cutting the semiconductor wafer along the cutting lines into chips; and

a step of providing interlayer connections among the semiconductor chips formed by the cutting step via the through electrodes that are cut by the cutting step.

19. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming trench sections on cutting lines of a semiconductor wafer having wiring layers formed thereon;

a step of forming dielectric films within the trench sections;

a step of forming an under barrier metal layer that covers the dielectric films and is connected to the wiring layers;

a step of thinning a back surface of the semiconductor wafer to thereby make the trench sections penetrate to form through holes along the cutting lines;

a step of cutting the semiconductor wafer along the cutting lines into chips;

a step of stacking the semiconductor chips formed by the cutting step; and

a step of filling conductive layers in the through holes that are divided by the cutting step.

20. A method for manufacturing a semiconductor module, characterized in comprising:

a step of forming through holes on cutting lines of a semiconductor wafer;

a step of cutting the semiconductor wafer along the cutting lines into chips;

a step of stacking the semiconductor chips on a interposer substrate having pin-like terminals standing thereon in a manner that the pin-like terminals are inserted in the through holes divided by the cutting step; and

a step of filling conductive layers in the through holes that are cut.

21. A method for manufacturing a semiconductor module, characterized in comprising:

a step of mounting semiconductor chips on interposer substrates having grooves formed in side walls thereof and recessed sections formed in back surfaces thereof;

a step of stacking the interposer substrates having the semiconductor chips mounted thereon in layers such that each of the semiconductor chips is stored in each of the recessed sections of an upper layer of the stacked interposer substrates; and

a step of filling conductive layers in the grooves of the interposer substrates to provide interlayer connections.

22. A method for manufacturing a semiconductor module, characterized in comprising:

a step of mounting semiconductor chips on interposer substrates having grooves formed in side surfaces thereof;

a step of stacking the interposer substrates having the semiconductor chips mounted thereon through intermediate substrates having opening sections formed in main surfaces thereof and grooves formed in side walls thereof; and

a step of filling conductive layers in the grooves of the interposer substrates and the intermediate substrates to provide interlayer connections.